Marwadi University
Faculty of Diploma studies
Information and Communication Technology

Subject Code : 09CT0510
Subject Name: VLSI
Diploma Year – III (Semester V)

Objective: The objective of the subject is to give an exposure to the VLSI design flow, CMOS digital logic circuits and introduction to HDL programming.

Credits Earned: 4

Course Outcomes: After learning this course, students should be able to,

1. Understand VLSI design flow
2. Learn CMOS fundamentals
3. Learn CMOS logic circuits
4. Develop programs for various circuits using HDL

Pre-requisite of course: Digital Electronics, Basic Electronics

Teaching and Examination Scheme

Teaching Scheme (Hours)			Credits	Theory Marks			Tutorial/ Practical Marks		Total Marks
Theory	Tutorial	Practical		ESE (E)	IA (M)	CSE (I)	Viva (V)	Term work (TW)	
3	0	2	4	50	30	20	25	25	150

Contents:

Unit No	Course content	Total Hrs.
1	**Introduction to VLSI Design** Historical perspective, VLSI design flow, Design Methodologies, Y-chart, Full custom design, standard cell based design, FPGA based design	04
2	**Manufacturing Process of CMOS digital IC** Silicon wafer, Photolithography, Simplified process sequences, process flow for fabrication of n-type MOS transistor, CMOS n-well process, Layout design rules	04
3	**MOS Transistor** MOS structure, MOS system under external bias and energy band diagram, Understanding accumulation, depletion and inversion,	07

	Structure and operation of MOS transistor, MOSFET current-voltage characteristics, MOSFET scaling, MOSFET capacitance	
4	**MOS Inverters** Voltage Transfer Characteristics(VTC) of Ideal inverter, Typical VTC of a realistic n-MOS inverter, Noise Immunity and Noise Margins, Resistive load inverter and its analysis, Inverter with n-Type MOSFET load(Enhancement-Load NMOS Inverter and Depletion-Load NMOS Inverter), CMOS Inverter	**07**
5	**Combinational MOS logic circuits** Two input NAND gate and NOR gate with depletion NMOS load, CMOS logic circuits, CMOS NOR(2-input) and CMOS NAND(2-input) gate, Complex logic circuits, CMOS Transmission gates	**07**
6	**Sequential MOS logic circuits** Introduction, CMOS SR latch based on 2-input NOR gates, CMOS SR latch based on 2-input NAND gates, Clocked SR latch, Clocked JK latch, JK Master-Slave flip-flops, CMOS D-latch and edge triggered D-flip-flop	**07**
7	**Introduction to HDL** Types of HDL, Describing hardware in HDL, basic concepts,behavioural design, structural design	**06**
	Total	**42 hrs.**

Suggested List of Experiments:

1. Write the HDL code for AND, OR and INV logic gates and do simulation.
2. Write the HDL code for NAND and NOR logic gates and do simulation.
3. Write the HDL code for XOR and XNOR logic gates and do simulation.
4. Write the HDL code for basic arithmetic circuits adder and subtractor. Do the simulation.
5. Write the HDL code for decoder circuits and do the simulation.
6. Write the HDL code for multiplexer circuit and do simulation.
7. Write the HDL code for encoder circuit and do simulation.
8. Write the HDL code for demultiplexer and do simulation.
9. Write the HDL code for SR latch and simulate.
10. Write the HDL code for D latch and simulate.
11. Write the HDL code for D flip-flop and simulate.
12. Write the HDL code for T flip-flop and simulate.
13. Write the HDL code for 4-bit register (Parallel in Parallel out) and simulate.
14. Write the HDL code for shift register and simulate.
15. Write the HDL code for up counter and down counter and simulate.

References:

1. CMOS Digital Integrated Circuits by Sung Mo Kang and Leblebici, TMH
2. Introduction to VLSI Circuits and Systems by Uyemura J P, Wiley India
3. Verilog HDL by Samir Palnitkar
4. VHDL modeling of systems by Znawabi, TMH

Suggested Theory distribution:

The suggested theory distribution as per Bloom's taxonomy is as per follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

R Level	U Level	A Level	N Level	E Level	C Level
30	**30**	**20**	**10**	**10**	**0**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)